See Remarks

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled)

Claim 2 (canceled)

Claim 3 (canceled)

Claim 4 (canceled)

Claim 5 (canceled)

Claim 6 (canceled)

Claim 7 (canceled)

Claim 8 (canceled)

Claim 9 (canceled)

Claim 10 (canceled)

Claim 11 (canceled)

Claim 12 (previously presented): A graphics controller integrated circuit for connection to a CPU and a display, said controller system comprising

a graphics engine for performing logic operations upon video data responsive to instructions from said CPU, said graphics engine having logic circuits formed from P-channel and N-channel transistors, said P-channel transistors having sources connected to a first voltage supply line, said N-channel transistors having sources connected to a second voltage supply line, and said N-channel transistors placed in a substrate region connected to a third voltage supply

line, said third voltage supply line at a negative voltage with respect to the voltage on said second voltage supply line;

a video memory holding said video data; and

a data interface between said graphics engine and said video memory to reduce power dissipation.

Claim 13 (previously presented): In an integrated circuit having a logic portion having at least 30K logic gates and a memory portion having a capacity of at least 2 megabits, a buffer circuit comprising

a PMOS transistor in an N-well and having a gate, first and second source/drains, said first source/drain connected to a first voltage supply line;

an NMOS drive transistor in a P-well and having a gate, first and second source/drains, said gate connected in common with said gate of said PMOS drive transistor to an input terminal, said second source/drain of said NMOS drive transistor connected in common with said second source/drain of said PMOS drive transistor to an output terminal, and said first source/drain connected to a second voltage supply line, said second voltage supply line at a negative voltage with respect to said first voltage supply line; and

a third voltage supply line connected to said P-well, said third voltage supply line at a negative voltage with respect to said second voltage supply line;

whereby a latch-up condition is avoided.

Claim 14 (previously presented): In an integrated circuit having a logic portion having at least 30 K logic gates and a memory portion having a capacity of at least 2 megabits, a buffer circuit having an output driver stage comprising

a PMOS drive transistor in an N-well and having a gate, first and second source/drains, said first source/drain connected to a first voltage supply line;

an NMOS drive transistor in a P-well and having a gate, first and second source/drains, said gate connected in common with said gate of said PMOS drive transistor to an input terminal, said second source/drain of said NMOS drive transistor connected in common with said second source/drain of said PMOS drive transistor to an output terminal, and said first source/drain

connected to a second voltage supply line, said second voltage supply line at a negative voltage with respect to said first voltage supply line; and

a third voltage supply line connected to said N-well through a tap near said PMOS drive transistor, said third voltage supply line at a positive voltage with respect to said first voltage supply line;

whereby a latch-up condition is avoided.

Claim 15 (previously presented): A complementary MOS integrated circuit having NMOS transistors and PMOS transistors, comprising

circuitry for processing, controlling or manipulating data of an electronic system which electronic system includes, or is interconnected with, said complementary MOS integrated circuit, said data processing, controlling or manipulating circuitry including at least 30K logic gates;

a memory for storing and retrieving at least a portion of said data, said memory having a capacity of at least 2 megabits; at least a portion of said data processing, controlling or manipulating circuitry isolated from said memory by at least one reverse-biased semiconductor junction between said data processing, controlling or manipulating circuitry and said memory; and

a data interface located between said data processing, controlling or manipulating circuitry and said memory, said data interface being at least 128 bits wide;

whereby the number of package pins, and the power dissipation, associated with implementing the functions performed by said data processing, controlling or manipulating circuitry, said memory and said data interface are reduced overall by integrating said data processing, controlling or manipulating circuitry, said memory and said data interface into said complementary MOS integrated circuit.

Claim 16 (previously presented): The complementary MOS integrated circuit of claim 15 wherein said at least a portion of said data processing, controlling or manipulating circuitry comprises a capacitor.

Claim 17 (previously presented): The complementary MOS integrated circuit of claim 16 wherein said capacitor comprises a PMOS transistor.

Claim 18 (previously presented): The complementary MOS integrated circuit of claim 15, wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 19 (previously presented): The complementary MOS integrated circuit of claim 15 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 20 (previously presented): The complementary MOS integrated circuit of claim 15 wherein said data processing, controlling or manipulating circuitry contains one or more analog circuits.

Claim 21 (previously presented): The complementary MOS integrated circuit of claim 20 wherein one or more of said one or more analog circuits consists mainly of PMOS transistors.

Claim 22 (previously presented): The complementary MOS integrated circuit of claim 20 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 23 (previously presented): The complementary MOS integrated circuit of claim 20 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 24 (previously presented): The complementary MOS integrated circuit of claim 15 wherein said data processing, controlling or manipulating circuitry portion has at least 40K logic gates and said memory has a capacity of at least 7.3 megabits.

Claim 25 (previously presented): The complementary MOS integrated circuit of claim 24 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 26 (previously presented): The complementary MOS integrated circuit of claim 24 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 27 (previously presented): The complementary MOS integrated circuit of claim 24 wherein said data processing, controlling or manipulating circuitry contains one or more analog circuits.

Claim 28 (previously presented): The complementary MOS integrated circuit of claim 27 wherein one or more of said one or more analog circuits consists mainly of PMOS transistors.

Claim 29 (previously presented): The complementary MOS integrated circuit of claim 16 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 30 (previously presented): The complementary MOS integrated circuit of claim 16 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 31 (previously presented): A complementary MOS integrated circuit having NMOS transistors and PMOS transistors in a semiconductor substrate, comprising

circuitry for processing, controlling or manipulating data of an electronic system which electronic system includes, or is interconnected with, said complementary MOS integrated circuit, said circuitry including at least 30K logic gates in said semiconductor substrate;

a memory for storing and retrieving at least a portion of said data, said memory having a plurality of transistors and capacitors in said semiconductor substrate and having a capacity of at least 2 megabits, at least a portion of said data processing, controlling or manipulating circuitry

isolated from said memory of transistors and capacitors by at least one reverse-biased semiconductor junction between said data processing, controlling or manipulating circuitry and said memory in said semiconductor substrate; and

a data interface located between said circuitry and said memory, said data interface being at least 128 bits wide;

whereby the number of package pins, and the power dissipation, associated with implementing functions performed by said data processing, controlling or manipulating circuitry, said memory and said data interface are reduced overall by integrating said data processing, controlling or manipulating circuitry, said memory and said data interface into said complementary MOS integrated circuit.

Claim 32 (previously presented): The complementary MOS integrated circuit of claim 31 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 33 (previously presented): The complementary MOS integrated circuit of claim 31 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 34 (previously presented): The complementary MOS integrated circuit of claim 31 further comprising

isolation circuitry to maintain said isolation by said at least one reverse-biased semiconductor junction.

Claim 35 (previously presented): The complementary MOS integrated circuit of claim 34 wherein said isolation circuitry comprises an on-chip bias generator.

Claim 36 (previously presented): The complementary MOS integrated circuit of claim 34 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 37 (previously presented): The complementary MOS integrated circuit of claim 34 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 38 (previously presented): The complementary MOS integrated circuit of claim 31 wherein said data processing, controlling or manipulating circuitry contains one or more analog circuits.

Claim 39 (previously presented): The complementary MOS integrated circuit of claim 38 wherein one or more of said one or more analog circuits consists mainly of PMOS transistors.

Claim 40 (previously presented): The complementary MOS integrated circuit of claim 38 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 41 (previously presented): The complementary MOS integrated circuit of claim 38 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 42 (previously presented): The complementary MOS integrated circuit of claim 34 wherein said data processing, controlling or manipulating circuitry contains one or more analog circuits.

Claim 43 (previously presented): The complementary MOS integrated circuit of claim 42 wherein one or more of said one or more analog circuits consists mainly of PMOS transistors.

Claim 44 (previously presented): The complementary MOS integrated circuit of claim 42 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 44 (cancel)

Claim 46 (previously presented): The complementary MOS integrated circuit of claim 31 wherein said data processing, controlling or manipulating circuitry has at least 40K logic gates and said memory has a capacity of at least 7.3 megabits.

Claim 47 (previously presented): The complementary MOS integrated circuit of claim 46 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 48 (previously presented): The complementary MOS integrated circuit of claim 46 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 49 (previously presented): The complementary MOS integrated circuit of claim 34 wherein said data processing, controlling or manipulating circuitry has at least 40K logic gates and said memory has a capacity of at least 7.3 megabits.

Claim 50 (previously presented): The complementary MOS integrated circuit of claim 49 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 51 (previously presented): The complementary MOS integrated circuit of claim 49 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 52 (previously presented): A complementary MOS integrated circuit having NMOS transistors and PMOS transistors, comprising

circuitry for processing, controlling or manipulating data of an electronic system which electronic system includes, or is interconnected with, said complementary MOS integrated circuit, said data processing, controlling or manipulating circuitry including at least 30K logic gates;

additional circuitry configured in such a way as to reduce the possibility of semiconductor junctions positioned within said complementary MOS integrated circuit between said processing, controlling or manipulating circuitry and said memory becoming forward biased;

a memory for storing and retrieving at least a portion of said data, said memory having a capacity of at least 2 megabits;

a data interface located between said data processing, controlling or manipulating circuitry and said memory, said data interface being at least 128 bits wide;

whereby integration of said data processing, controlling or manipulating circuitry, said additional circuitry, said memory and said data interface into a single complementary MOS integrated circuit reduces overall package pin count.

Claim 53 (previously presented): The complementary MOS integrated circuit of claim 52 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 54 (previously presented): The complementary MOS integrated circuit of claim 52 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 55 (previously presented): The complementary MOS integrated circuit of claim 52 wherein said data processing, controlling or manipulating circuitry contains one or more analog circuits.

Claim 56 (previously presented): The complementary MOS integrated circuit of claim 55 wherein one or more of said one or more analog circuits consists mainly of PMOS transistors.

Claim 57 (previously presented): The complementary MOS integrated circuit of claim 55 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 58 (previously presented): The complementary MOS integrated circuit of claim 55 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 59 (previously presented): The complementary MOS integrated circuit of claim 52 wherein said data processing, controlling or manipulating circuitry has at least 40K logic gates and said memory has a capacity of at least 7.3 megabits.

Claim 60 (previously presented): The complementary MOS integrated circuit of claim 59 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU.

Claim 61 (previously presented): The complementary MOS integrated circuit of claim 59 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.

Claim 62 (new): The complementary MOS integrated circuit of claim 42 wherein said data processing, controlling or manipulating circuitry, said memory and said data interface are configured in such a way as to communicate with a CPU through a CPU interface.